Code No: **R42046** **R10** **Set No. 1**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2015

STRUCTURED DIGITAL DESIGN

(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1 a) Explain top-down Design methodology with example. [8]

b) Explain the need for hardware description languages with examples. [7]

2 a) Distinguish between the following
i) Function Vs Procedure ii) signals vs. variables [8]

b) Explain the utilities of package declaration and package body with suitable examples. [7]

3 a) Design a 4:16 decoder using structural modelling and write a VHDL code for it [8]

b) Write VHDL code for 4:1 multiplexer using 2:1 multiplexers. [7]

4 a) Implement a MOD 6 up/down counter using VHDL and also write the test bench for it. [8]

b) Implement a 4 bit shift register using VHDL. [7]

5 a) Design verilog module for 4 bit carry look ahead full adder. [8]

b) Implement a 1 to 4 demultiplexer by using 2 to 4 decoder with verilog module. [7]

6 a) Write a Verilog function that will accept two 8-bit inputs, data_in, and address, and print out the values in hexadecimal format. [8]

b) Write a verilog code for master slave JK flip flop using NAND gates. [7]

7 a) Explain the synthesis of Edge-Triggered Flip-Flops. [8]

b) Explain the synthesis of tristate buffer in detail. [7]

8 a) Explain logic fault models of stuck at faults and bridging faults. [8]

b) Explain controllability and observability with suitable example. [7]

Code No: **R42046** **R10** **Set No. 2**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2015

STRUCTURED DIGITAL DESIGN

(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
****

1	a)	Explain different phases in physical design of a digital system.	[8]
	b)	Define both simulation and synthesis with respect to design considerations and also explain the available simulation and synthesis tools.	[7]
2	a)	Explain delta delay, inertial delay and transport delay with suitable examples.	[8]
	b)	Explain different VHDL operators with suitable examples.	[7]
3	a)	Write a VHDL code using generate statement to convert binary to gray code converter.	[8]
	b)	With the state graph of binary multiplier control, write the behavioral model for 4 x 4 binary multiplier using VHDL.	[7]
4	a)	Design a Moore finite state machine that acts as a "101" sequence detector using VHDL in behavioural model.	[8]
	b)	Write a VHDL function that converts a 5-bit bit vector to an integer.	[7]
5	a)	Write a verilog code for converting a binary number to a real number.	[8]
	b)	Implement a serial adder using Verilog modules.	[7]
6	a)	Implement a 4-bit parallel shift register using Verilog.	[8]
	b)	Write the Verilog code for four bit up counter with parallel load.	[7]
7	a)	Explain the steps involved in synthesis process.	[8]
	b)	Explain the synthesis of edge triggered Flip Flops.	[7]
8	a)	What are different stuck at faults and explain how these faults are identified with appropriate test vectors.	[8]
	b)	Draw the architecture of a Built In Self Test (BIST) and explain the functions to be carried out by BIST controller during testing.	[7]

Code No: **R42046** **R10** **Set No. 3**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2015

STRUCTURED DIGITAL DESIGN

(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1 a) Explain the steps involved in designing a system using CAD tools with the help of a flow graph. [8]
b) Explain the different levels of modelling with suitable examples. [7]

2 a) Explain about data objects in VHDL programming. [8]
b) What is binding? Discuss binding between
i) Entity and architecture ii) Entity and components [7]

3 a) Write VHDL description of an N bit ripple carry adder using procedure. [8]
b) Design a 9-bit parity generator circuit using structural modelling style. [7]

4 a) Using D-type flip flops, design a synchronous Mealy finite-state machine that monitors binary input A and asserts a binary output B if the sequence 100 is observed. [8]
b) Write VHDL code for a D-latch using variable and signal assignment statements. Also clearly distinguish between the 2 statements with simulation waveforms. [7]

5 a) Implement 3 bit magnitude comparator in structural style using Verilog. [8]
b) Implement a 32 bit unsigned integer multiplier using Verilog. [7]

6 a) Explain the design of a Keypad scanner using Verilog. [8]
b) Design a linear feedback shift register using Verilog Dataflow model. [7]

7 a) Distinguish between the synthesis of explicit and implicit state machines. [8]
b) Distinguish between Behavioural synthesis and RTL synthesis, and explain about them with suitable examples. [7]

8 a) What are different stuck at faults and explain how these faults are identified with appropriate test vectors. [8]
b) Explain automated test pattern generation for single stuck faults for combinational circuits. [7]

Code No: **R42046** **R10** **Set No. 4**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2015

STRUCTURED DIGITAL DESIGN

(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1 a) Explain in detail about modelling of digital circuits at logic level and register level. [8]
b) Explain the components of a verilog Module with a neat block diagram. [7]

2 a) Explain various predefined operators in VHDL. [7]
b) Implement a 4-bit parallel adder circuit using VHDL in structural style. [8]

3 a) Write the VHDL code for an 8-bit counter employing D flip-flops using structural style of modelling. [8]
b) Design an 8-bit shift register using D-flip-flops and write the VHDL code for the same. [7]

4 a) Design a Mealy sequence detector using VHDL that detects a sequence of four consecutive 1 inputs. The detector has a single binary input, X, and a single binary output, Z. Signal Z should be logic 1 if and only if the last four inputs were all logic 1. [8]
b) Write a VHDL code for finding the word with the lowest ASCII value using. file operations. [7]

5 a) Implement a 4x16 decoder using 2x4 decoders as modules with verilog code. [8]
b) Write a Verilog code for Booth algorithm to find the product of two 4 bit numbers -3 and 8. [7]

6 a) Implement a 8-bit barrel shifter using the Verilog code. [8]
b) Design a modulo-12 up synchronous counter using T- flip flops and write the verilog code. [7]

7 a) Distinguish between the synthesis of combinational logic and sequential logic with suitable examples. [8]
b) Explain the synthesis of counters with suitable example. [7]

8 a) Explain the principle of operation of path sensitizations method with an example. [8]
b) Explain the importance of test pattern generation in BIST circuits. [7]